IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 13, Issue 1 Ver. III (Jan. – Feb. 2018), PP 01-09
www.iosrjournals.org

Generalized PWM Control of Dual Inverter Fed Induction Motor Drive

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Abstract: *A simplified generalized pulse width modulation (GPWM) algorithm is proposed to obtain various continuous and discontinuous PWM algorithms for a four level inverter topology. Induction motor both sides are fed with a three-level inverter from one side and a two-level inverter from the other side. The proposed configuration is capable to produce an output voltage of two-level, three-level and four-level in entire modulation range. Neutral clamping diodes and neutral point fluctuations are absent in the proposed inverter topology. In the proposed inverter topology the switching losses are reduced with the application of various discontinuous PWM algorithms compared with continuous PWM algorithms. Simulation analyses are carried out in MATLAB/SIMULINK environment and the results are presented.*
Keywords -*Generalized PWM, Space Vector PWM, Multi-level Inverter, Induction motor*

Date of Submission: 15-01-2018 Date of acceptance: 03-02-2018

I. Introduction

At present, voltage source converters are mostly used in adjustable speed electric drives. Pulse width modulation (PWM) techniques are employed to control the output voltage and frequency of Voltage Source Inverter (VSI). The switching manner employed in PWM techniques reduces harmonics in the output voltage. Based on switching fashion different PWM techniques are proposed in literature [1-4]. Among various PWM techniques space vector pulse width modulation (SVPWM) technique proposed in [4-5] gives superior performance for a voltage source inverter. In the conventional SVPWM algorithm, the zero vector time (T_z) is divided equally among the two possible zero states. The calculation of switching times (T_1, T_2 and T_z) require angular information and magnitude of reference voltage at each instant, which makes the SVPWM complex.

$$\begin{aligned} T_1 &= \frac{2\sqrt{3}}{\pi} M_i \sin(60^o - \alpha)\, T_s \\ T_2 &= \frac{2\sqrt{3}}{\pi} M_i \sin(\alpha) T_s \\ T_z &= T_s - T_1 - T_2 \end{aligned} \quad (1)$$

Where M_i is the modulation index $M_i = \frac{\pi V_{ref}}{2V_{dc}}$.

In [4], a simplified algorithm is proposed where no need to calculate the angular information by using the concept of imaginary switching times. Various discontinuous PWM algorithms have been pressed in [6-7] by the unequal division of zero state time along with simplification algorithms.The two level inverters induce more harmonic distortion. As the switching frequency increases the harmonic content in line current gets reduced. In order to obtain low harmonic distortion at low switching frequency multi-level inverter topologies are employed. Different multi-level topologies are introduced in literature[8-11]. Traditional multilevel inverter topologies like diode clamped and H-bridge topologies require clamping diodes, separate DC-link voltage sources. These multilevel topologies have the drawbacks of neutral point fluctuations and complexity increases as the number of levels increases. Cascade and dual inverter topologies are introduced to overcome these drawbacks and complexity. Two two-level inverter topologies are cascaded to generate three level output voltage, this configuration is called cascade inverter topology proposed in literature[12]. In similar fashion two two-level inverter configuration is proposed in literature[13]. Both cascade and dual inverter topologies are combined shown in Fig.1 to generate four-level output voltage.

In this paper, a simple and more generalized approach is introduced to generate all possible continuous and discontinuous PWM (DPWM) signals by adding a zero sequence voltage to the refence signals. The harmonic content in the output voltage is low at low switching frequency by employing proposed topology. Switching losses can also be reduced by employing various DPWM algorithms.

II. Proposed Inverter Topology

In the proposed inverter topology, an open-end winding induction motor is fed by a 3-level cascade inverter(two 2-level inverters are connected in cascade) from one end and 2-level inverter from the other end as shown in Fig.1. To control the output voltage and frequency of the inverter topology, various carrier based PWM algorithms are introduced. In multilevel inverter topologies to generate N-level output voltage (N-1) level shifting triangles are required.

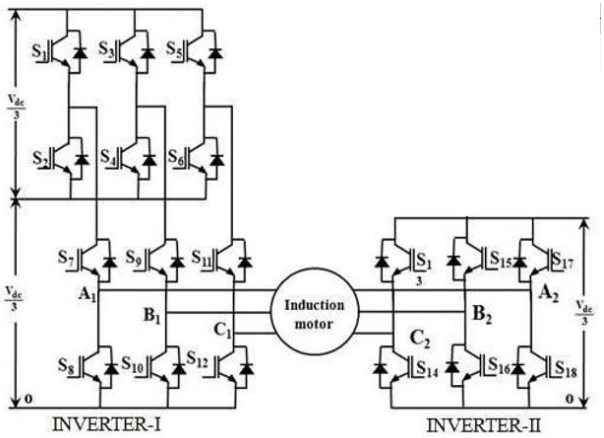

Fig.1 Proposed Inverter Topology

$V_{A1o}, V_{B1o}, V_{C1o}$represents the pole voltage of Inverter I.As two inverters are cascaded, Inverter I can generate three level output voltage.$V_{A2o}, V_{B2o}, V_{C2o}$ are the pole voltages of Inverter-II. The combined pole voltage of proposed multi-level inverter are given by

$$V_A = V_{A1o} - V_{A2o}$$
$$V_B = V_{B1o} - V_{B2o} \quad (2)$$
$$V_C = V_{C1o} - V_{C2o}$$

So to generate four-level output, three level shifting triangles are required. These level shifting triangles are divided into three regions R1, R2 and R3 as given in Fig.2.

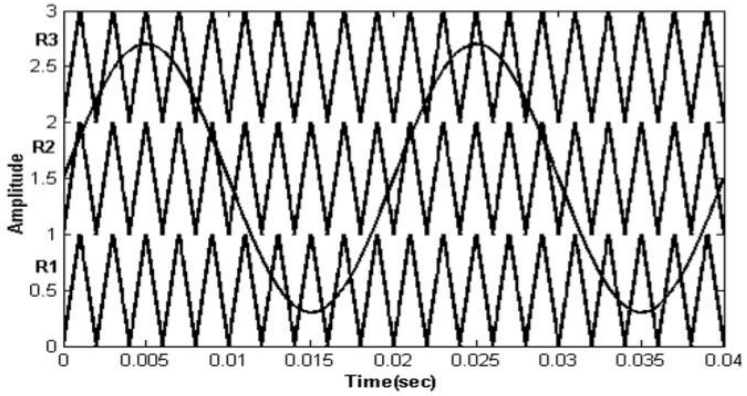

Fig. 2. Different regions in carrier comparison approach

V_c be the triangle wave amplitude and V_m be the reference wave amplitude. Now modulation index is defined as

$$M_i = \frac{V_m}{V_c(N-1)} \quad (3)$$

If the modulation signal lies within the region R1 as shown in Fig. 3, only Inverter-I is in operation and inverter-II is clamped.

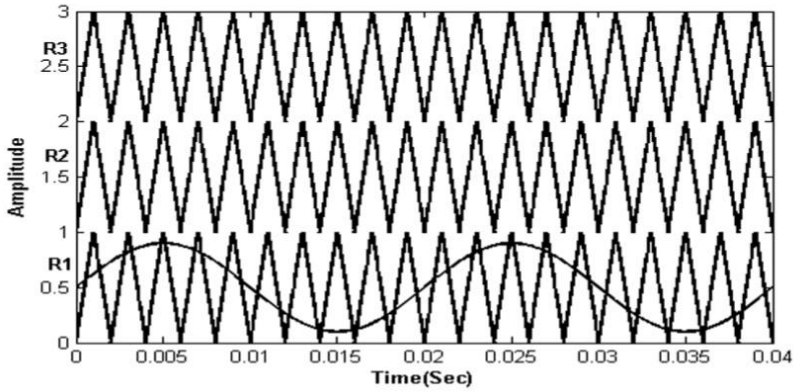

Fig. 3. Modulating signal position (R1) during two-level operation.

All the phases of inverter-I produces a two-level output voltage (Vdc/3 or 2Vdc/3) by operating switches (S1, S3, S5) and (S2, S4, S6) and clamping the switches (S7, S9, S11) to a voltage of positive voltage of Vdc/3. As the combined pole voltage of the proposed inverter produces two-level output the mode of operation is called as two-level operation. If the modulating wave is present in both regions R1 and R2 as shown in Fig. 4, all the switches in inverter-I operate continuously to produce output voltage. When switches (S1, S3, S5) and (S7, S9, S11) are ON Inverter-I produces an output voltage of (2Vdc/3). When (S2, S4, S6) and (S7, S9, S11) are ON inverter-I produces an output voltage of (Vdc/3). When (S8, S10, S12) are ON, inverter-I produces zero output voltage. Similarly, all the switches in inverter-II are clamped to produce a zero voltage.

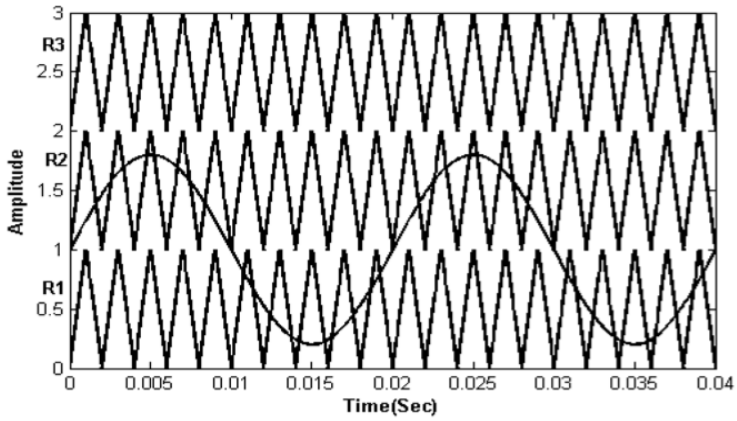

Fig. 4. Modulating signal position (R1,R2) during three-level operation.

Therefore the effective pole voltage of proposed multilevel inverter contains three levels (2Vdc/3, Vdc/3, 0). So this mode of operation is known as three-level mode of operation. When the modulating signal is present in all the three regions as shown in Fig.2 all the switches in proposed multilevel inverter topology operate continuously to produce an output voltage. During this mode of operation inverter-I produce three-level output voltage and inverter-II produce two-level output voltage. The corresponding pole voltages of inverter-I and inverter-II during this mode of operation are given in Table-1 along with their effective pole voltages. Thus a three phase induction motor attains four-level output voltages.

Table 1 Different voltages during four-level operation

Pole Voltage of INV-I V_{a10}	0	0	$V_{dc}/3$	$V_{dc}/3$	$2\,V_{dc}/3$	$2\,V_{dc}/3$
Pole Voltage of INV-II V_{a20}	0	$V_{dc}/3$	0	$V_{dc}/3$	0	$V_{dc}/3$
Effective Pole Voltage V_a	0	$-V_{dc}/3$	$+V_{dc}/3$	0	$+2\,V_{dc}/3$	$+V_{dc}/3$

The advantage of the proposed multilevel inverter topology is that all the four levels of operation can be achieved in entire modulation index (from 0 to 1).

III. Proposed Generalisedpwm Algorithm

Let us assume two sets of instantaneous phase voltages as given in equations (4) and (5).

$$\begin{aligned} V_{an} &= V_m \cos(wt) \\ V_{bn} &= V_m \cos(wt - 120) \\ V_{cn} &= V_m \cos(wt - 240) \end{aligned} \tag{4}$$

$$\begin{aligned} V_{ax} &= V_m \cos(wt) \\ V_{bx} &= V_m \cos(wt - 120) \\ V_{cx} &= V_m \cos(wt - 240) \end{aligned} \tag{5}$$

In the proposed generalized pulse width modulation (GPWM) algorithm, the potential at O and O' are isolated. The modulating waves are generated by simply adding zero sequence voltage to the instantaneous phase voltages as given in (6).

$$V_{in}^{*} = V_{in} + V_{zs}, \quad i = a, b, c \tag{6}$$

Where $$V_{zs} = \frac{V_{dc}}{2}(2a_0 - 1) - a_0 V_{max} + (a_0 - 1) \tag{7}$$

V_{zs} is known as zero sequence voltage.

V_{max} is the maximum of V_{an}, V_{bn}, V_{cn} and $V_{max,x}$ is the maximum value of V_{ax}, V_{bx}, V_{cx} in each sampling time interval. For the generation of various PWM algorithms, the variation of the constant is shown in Table-2 and the corresponding modulating signals are shown in Fig. 5. From the Fig. 5, it can be observed that the SVPWM has continuous modulating waveform and hence gives continuous pulse pattern. Whereas, the modulating waves of discontinuous PWM (DPWM) algorithms clamp to either positive dc or negative dc bus for a duration of 120 degrees in each fundamental cycle.

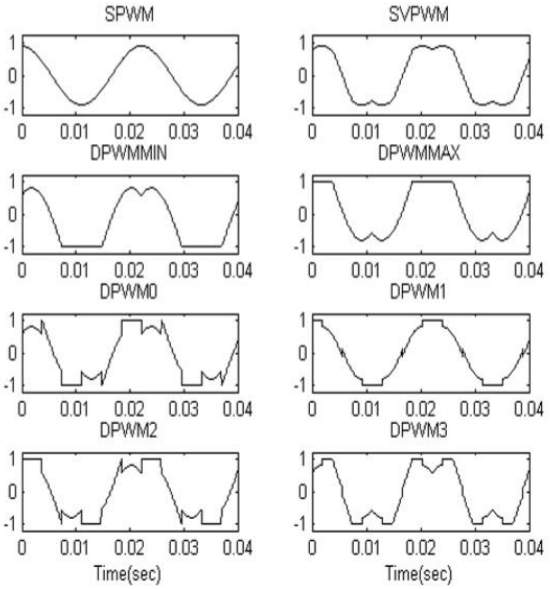

Fig. 5. Modulating signals of different PWM algorithms

Table 2 Various PWM algorithms for different values of a_0

PWM Algorithm	A_0
SVPWM	0.5
DPWMMIN	0
DPWMMAX	1
DPWM0	$V_{max} + V_{min} < 0$ *then* $a_0 = 0$ $V_{max} + V_{min} \geq 0$ *then* $a_0 = 1$
DPWM1	$V_{max\,x} + V_{min\,x} < 0$ *then* $a_0 = 0$ $V_{max\,x} + V_{min\,x} \geq 0$ *then* $a_0 = 1$
DPWM2	$V_{max} + V_{min} < 0$ *then* $a_0 = 1$ $V_{max} + V_{min} \geq 0$ *then* $a_0 = 0$
DPWM3	$V_{max\,x} + V_{min\,x} < 0$ *then* $a_0 = 0$ $V_{max\,x} + V_{min\,x} \geq 0$ *then* $a_0 = 1$

IV. Simulation Results And Discussion

The characteristics of multilevel inverter topology with different PWM algorithms have been studied and analyzed in MATLAB/simulation environment for a three phase induction motor. For the simulation studies, the switching frequency is taken as 3 kHz. Hence, the sampling time period (T) for is taken as 0.333ms. The simulation studies have been carried out for four-level operation. Hence, to achieve four -level operation, for a sampling time period of T inverter-I is switched for a period of (2T/3) and inverter-II is switched for a period of (T/3). Moreover, when one inverter is switched other inverter is clamped. The operation of inverters for various PWM algorithms is as shown in Table-3. The simulation results for various PWM algorithms for a four-level operation are shown in from Fig. 6 to Fig. 12.The induction motor parameters used in the analysis and inverter parameters are given in Table-4.

Table 3 Inverter Operation for various PWM algorithms

Type of PWM	Operation of Inverter I in 2T/3 time	Operation of Inverter I in T/3 time	Reason
SVPWM	Continuous Switching in 2T/3 Time	Continuous Switching in T/3 Time	Continuous modulating waveform
DPWMMIN	Clamped for some time duration in 2T/3 period	Continuous Switching in T/3 Time	As the modulating wave is clamped to negative dc bus
DPWMMAX	Continuous Switching in 2T/3 Time	Clamped for some time duration in T/3 period	As the modulating wave is clamped to negative dc bus
DPWM0	Clamped for some time duration in 2T/3 period	Clamped for some time duration in T/3 period	As the modulating wave is clamped to negative dc bus

Table 4 Parameters of the Induction Motor

Rated Speed	1500 RPM
Frequency	50 Hz
Stator Resistance	1.57Ω
Rotor Resistance	1.21Ω
Stator Inductance	183 mH
Rotor Inductance	183 mH
Mutual Inductance	176 mH
Inverter Input DC voltage	450 V

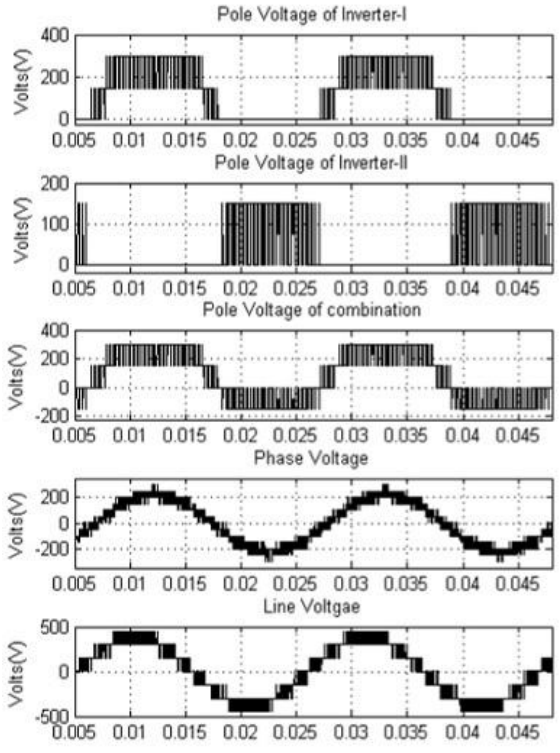

Fig. 6. Voltage plots with SVPWM during four-level operation

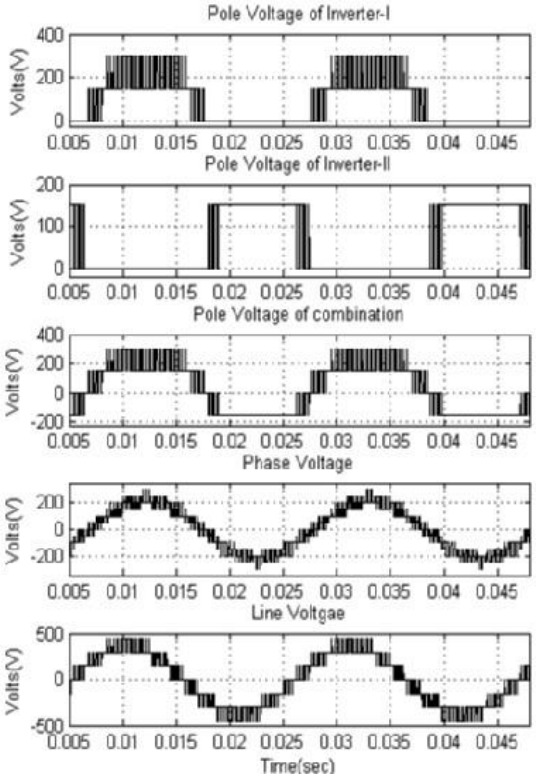

Fig. 7. Voltage plots with DPWMMAX during four-level operation

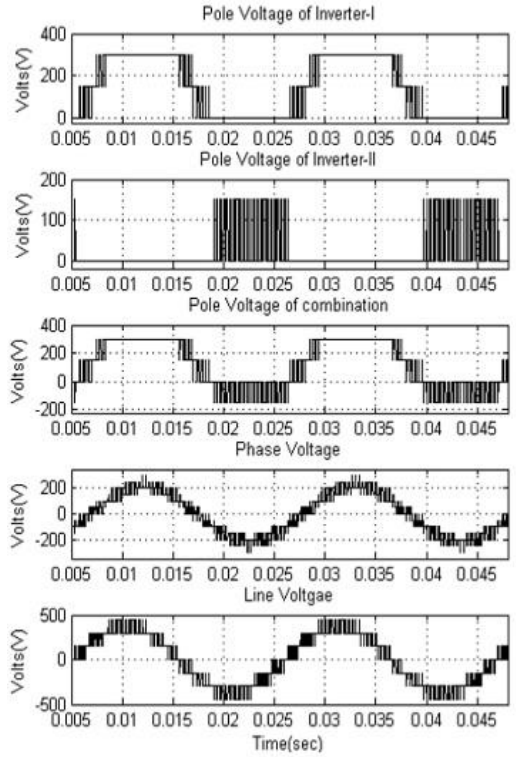

Fig. 8. Voltage plots with DPWMMIN during four-level operation

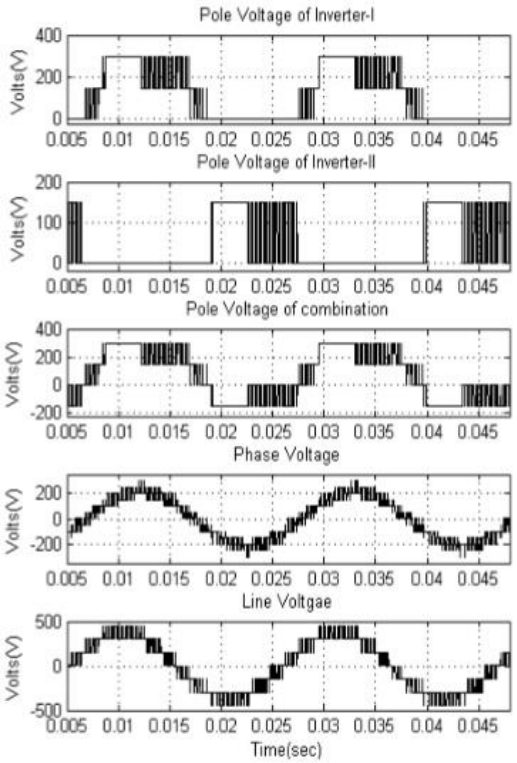

Fig. 9. Voltage plots with DPWM0 during four-level operation

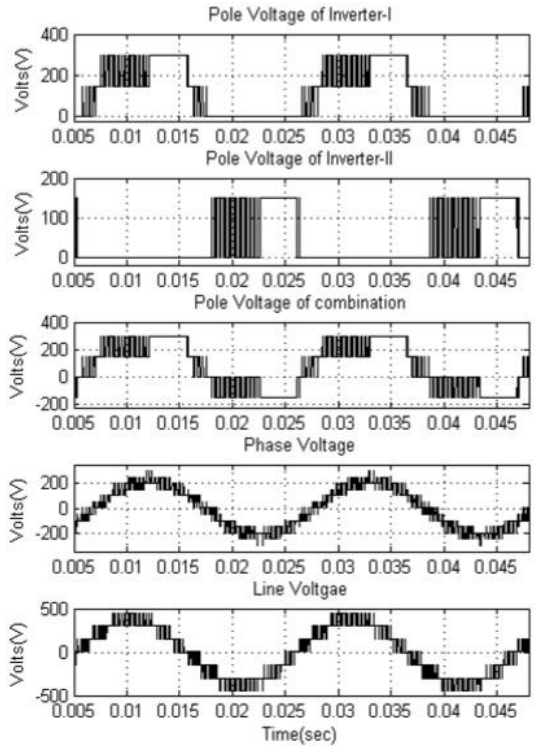

Fig. 10. Voltage plots with DPWM2 during four-level operation

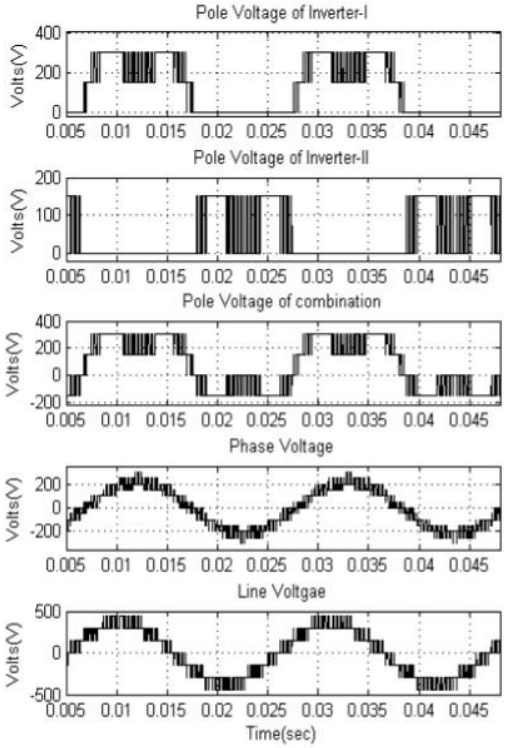

Fig. 11. Voltage plots with DPWM3 during four-level operation

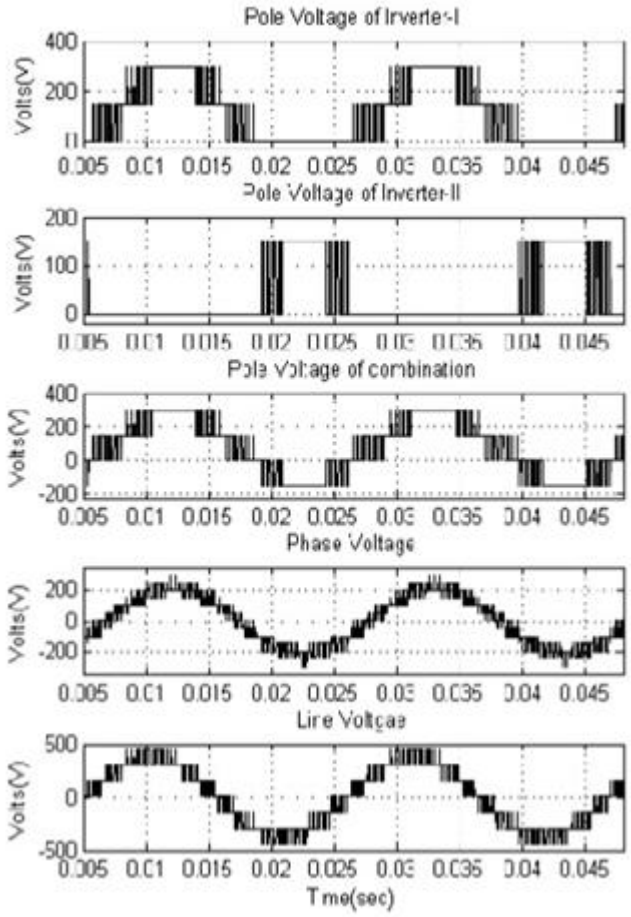

Fig. 12. Voltage plots with DPWM1 during four-level operation

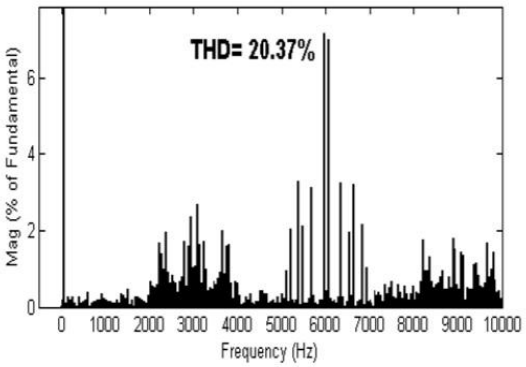

Fig. 13. Harmonic spectra of line voltage for SVPWM algorithm

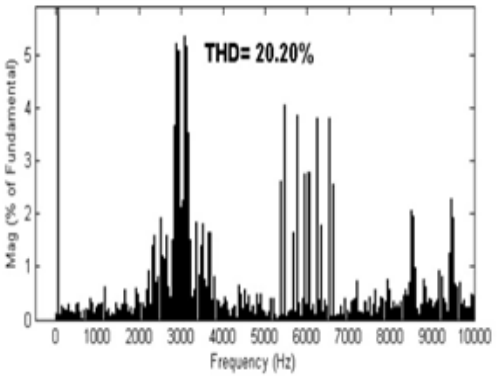

Fig. 14. Harmonic spectra of line voltage for DPWM1 algorithm

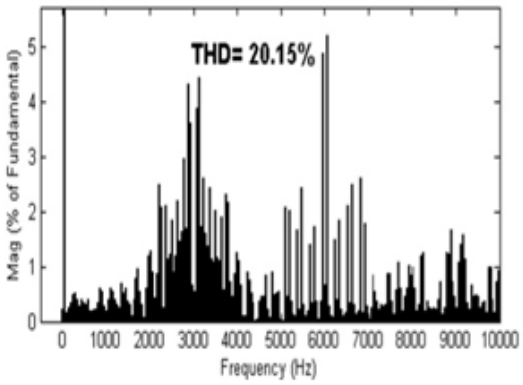

Fig. 15. Harmonic spectra of line voltage for DPWM2 algorithm

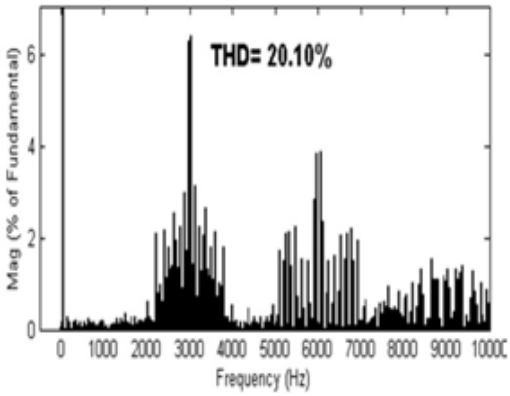

Fig. 16. Harmonic spectra of line voltage for DPWMAX algorithm

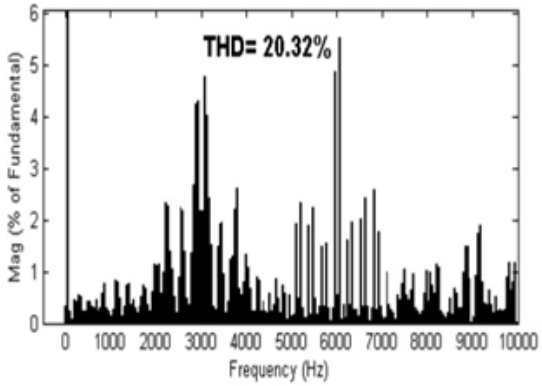

Fig. 17. Harmonic spectra of line voltage for DPWM3 algorithm

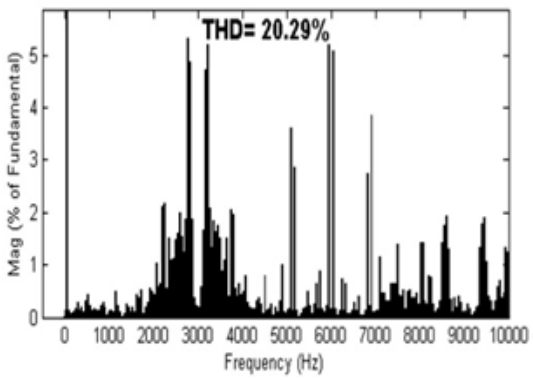

Fig. 18. Harmonic spectra of line voltage for DPWM0 algorithm

The harmonic spectra of line voltages for various PWM algorithms are shown in from Fig. 13 to Fig. 18 for four-level operation. From the harmonic spectra results, it can be observed that as the number of levels increases, the harmonic distortion also decreases. Moreover, the proposed GPWM algorithm gives all possible PWM algorithms with reduced complexity. And, also it can be concluded that as the DPWM algorithms clamp for a total period of 120 degrees in each fundamental cycle, the switching losses can be reduced 33.33%.

V. Conclusion

The proposed GPWM algorithm is simple and less complex when compared to conventional PWM algorithms. From the results, it can be concluded that discontinuous PWM techniques reduce a total of 33% of switching losses when compared to continuous PWM algorithms. The proposed inverter topology can generate two-level, three-level and four-level output voltages with reduced switching losses at all the modulation indices. As the number of levels increase harmonic content in the output voltage gets reduced. In view of performance, the proposed inverter topology is highly efficient at low voltage rating also. During faulty conditions of the drive, the complete motor drive can be operated with one set of the inverter by isolating another inverter from the operation.

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IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) is UGC approved Journal with Sl. No. 4198, Journal no. 45125.

B Ravichandra Rao "Generalized PWM Control of Dual Inverter Fed Induction Motor Drive." IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) 13.1 (2018): 01-09.